

Hardware Unit Test Report

Set-Top Box

T99X171T00

IIC Timing test

Hardware version	Kernel version	Sample No.	eMMC P/N
V005	4.9.113 #2 Wed Jan 30 17:12:43 CST 2019	S/N:	KLM8G1GETF-B041

1. HDMI Output Port DDC I2C Bus Timing Test

1.1 I2C bus timing specification

Table 3-21 Summary of I²C support

Applicable standard	Feature exceptions	MPQ variations
I ² C Specification, version 2.1, January 2000 (Philips Semiconductor document number 9398 393 40011)	Clock stretching is available.	None

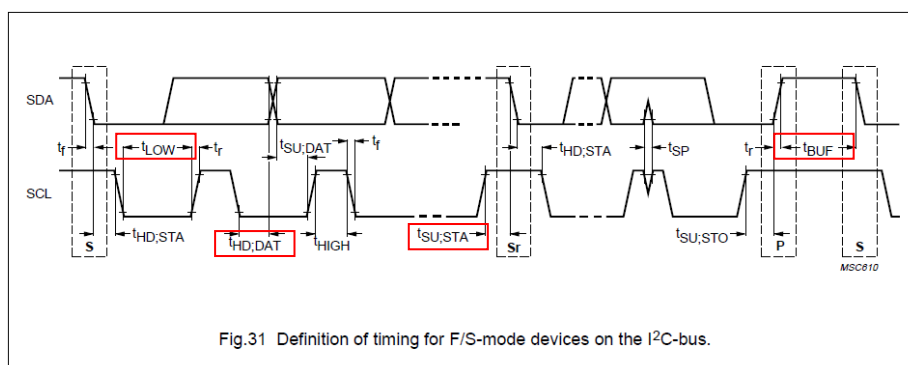


Fig.31 Definition of timing for F/S-mode devices on the I²C-bus.

Table 5 Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices⁽¹⁾

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f _{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD;STA}	4.0	–	0.6	–	μs
LOW period of the SCL clock	t _{LOW}	4.7	–	1.3	–	μs
HIGH period of the SCL clock	t _{HIGH}	4.0	–	0.6	–	μs
Set-up time for a repeated START condition	t _{SU;STA}	4.7	–	0.6	–	μs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I ² C-bus devices	t _{HD;DAT}	5.0 0 ⁽²⁾	– 3.45 ⁽³⁾	– 0 ⁽²⁾	– 0.9 ⁽³⁾	μs μs
Data set-up time	t _{SU;DAT}	250	–	100 ⁽⁴⁾	–	ns
Rise time of both SDA and SCL signals	t _r	–	1000	20 + 0.1C _b ⁽⁵⁾	300	ns
Fall time of both SDA and SCL signals	t _f	–	300	20 + 0.1C _b ⁽⁵⁾	300	ns
Set-up time for STOP condition	t _{SU;STO}	4.0	–	0.6	–	μs
Bus free time between a STOP and START condition	t _{BUF}	4.7	–	1.3	–	μs
Capacitive load for each bus line	C _b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V _{nL}	0.1V _{DD}	–	0.1V _{DD}	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{nH}	0.2V _{DD}	–	0.2V _{DD}	–	V

1.2 Measurement result and picture

Measure points are at R1403/R1404 for HDMI_SCL/ HDMI_SDA.

SYMBOL	Specification		UNIT	Result	Pass/Fail	Figure
	MIN	MAX				
f _{SCL}	0	100	KHz	51.12K	Pass	1.2a
t _{HD;STA}	4	-	us	8.84	Pass	1.2b
t _{LOW}	4.7	-	us	10.76	Pass	1.2c
t _{HIGH}	4.0	-	us	8.84	Pass	1.2d
t _{SU;STA}	4.7	-	us	9.16	Pass	1.2e
t _{HD;DAT}	0	3.45	us	0.76	Pass	1.2f
t _{SU;DAT}	250	-	ns	9960	Pass	1.2g
t _{SU;STO}	4	-	us	9.52	Pass	1.2h
t _{BUF}	4.7	-	us	2978	Pass	1.2i

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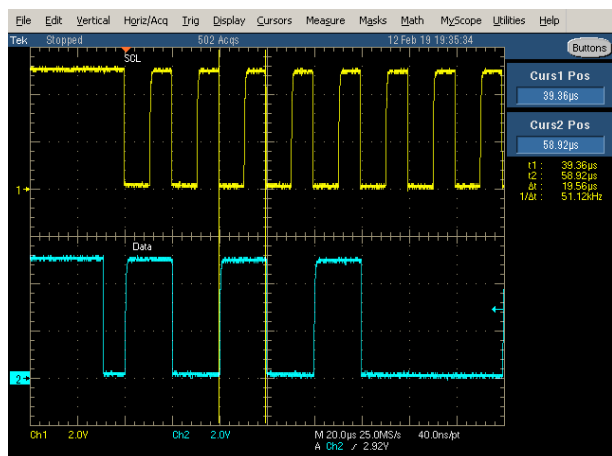


Figure 1.2a: fSCL

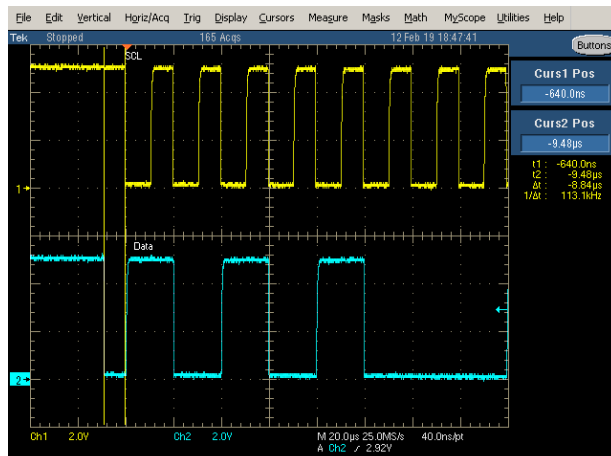


Figure 1.2b: tHD;STA

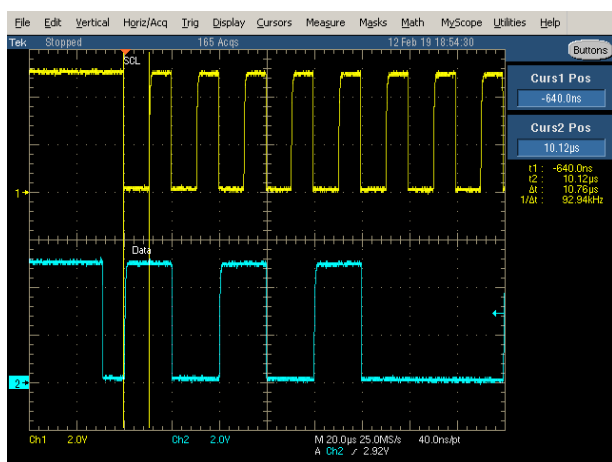


Figure 1.2c: tLOW

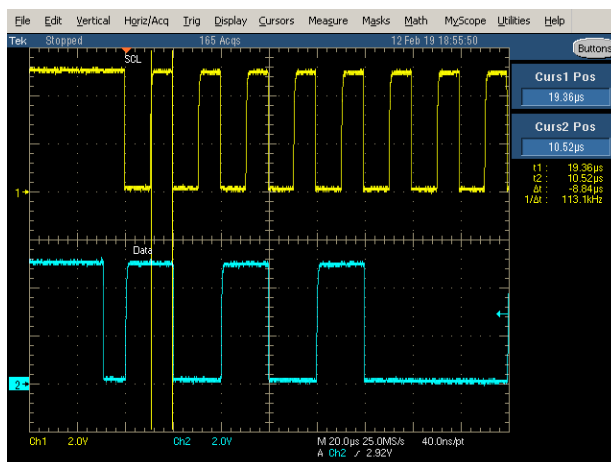


Figure 1.2d: tHIGH

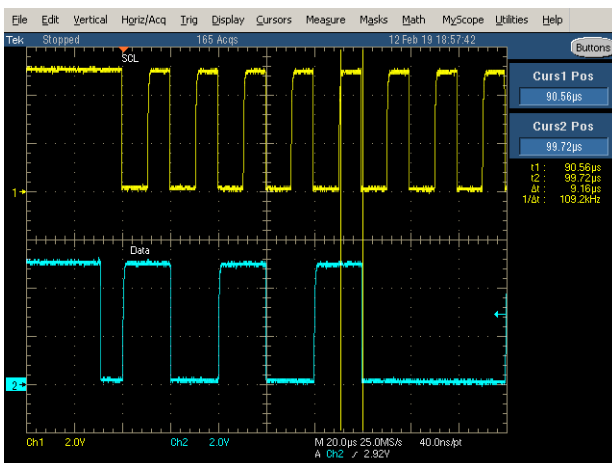


Figure 1.2e: tSU;STA

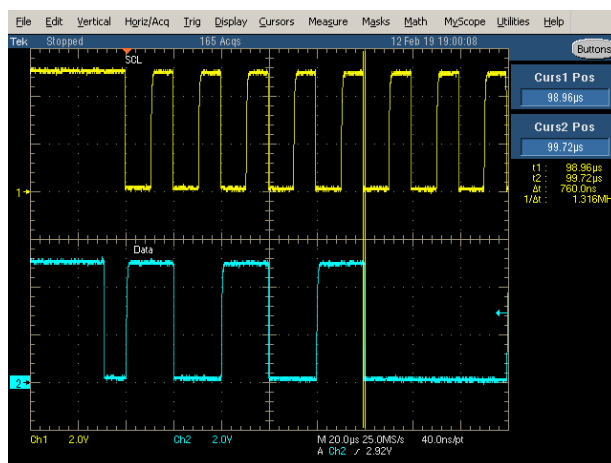


Figure 1.2f: tHD;DAT

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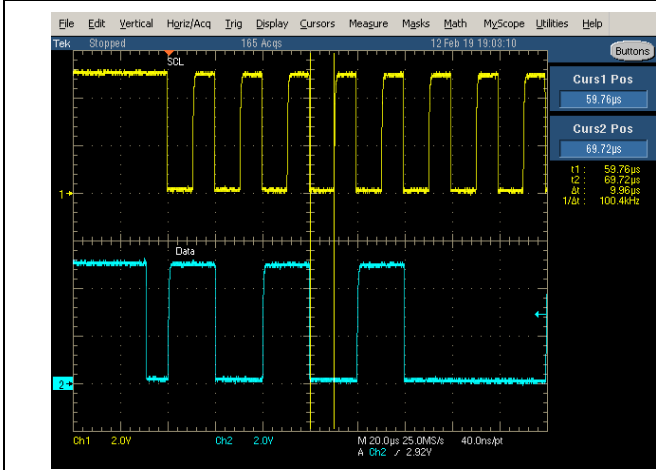


Figure 1.2g: tSU;DAT

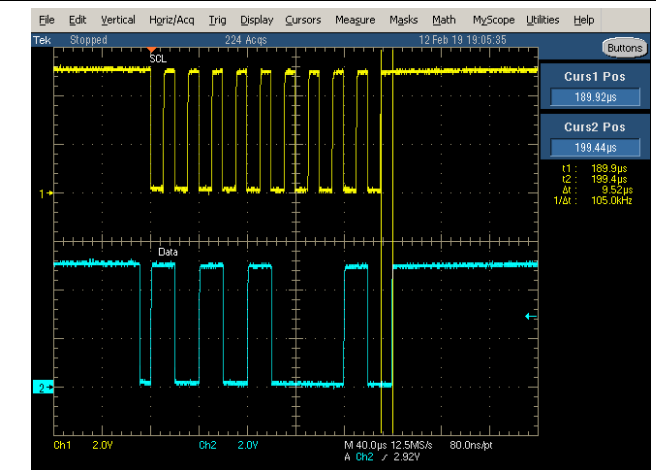


Figure 1.2h: tSU;STO

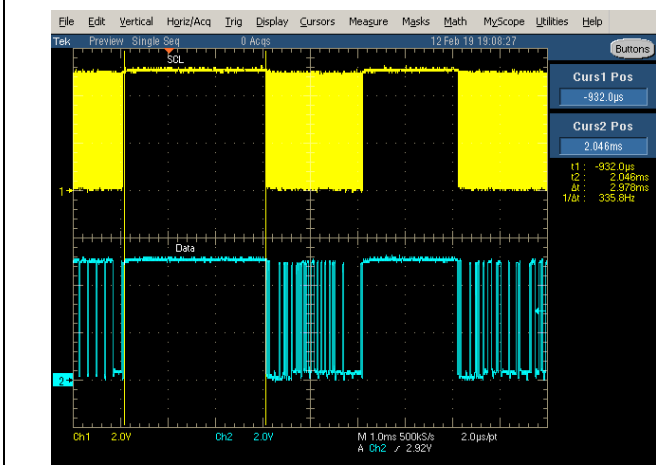


Figure 1.2i: tBUF

2. ADC I2C Bus Timing Test

2.1 I2C bus command: SoC to ADC (U1101: TLV320ADC3101IRGET)

The command from SoC to ADC to capture MIC:

tinycap /data/test.wav -D 0 -d 1 -r 48000

Note: needs to use “su” command to enter, the commands for i2c can run.

2.2 I2C bus timing specification

Table 3-21 Summary of I²C support

Applicable standard	Feature exceptions	MPQ variations
I ² C Specification, version 2.1, January 2000 (Philips Semiconductor document number 9398 393 40011)	Clock stretching is available.	None

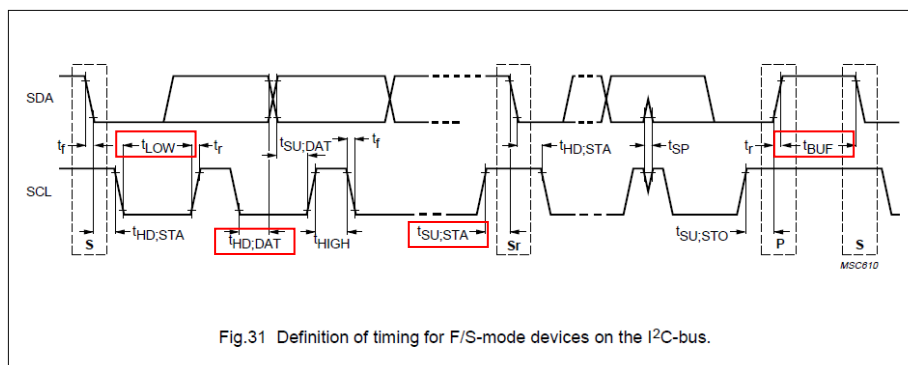


Table 5 Characteristics of the SDA and SCL bus lines for F/S-mode I²C-bus devices⁽¹⁾

PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD,STA}$	4.0	—	0.6	—	μs
LOW period of the SCL clock	t_{LOW}	4.7	—	1.3	—	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	—	0.6	—	μs
Set-up time for a repeated START condition	$t_{SU,STA}$	4.7	—	0.6	—	μs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I ² C-bus devices	$t_{HD,DAT}$	5.0 0 ⁽²⁾	— 3.45 ⁽³⁾	— 0 ⁽²⁾	— 0.9 ⁽³⁾	μs μs
Data set-up time	$t_{SU,DAT}$	250	—	100 ⁽⁴⁾	—	ns
Rise time of both SDA and SCL signals	t_r	—	1000	$20 + 0.1C_b^{(5)}$	300	ns
Fall time of both SDA and SCL signals	t_f	—	300	$20 + 0.1C_b^{(5)}$	300	ns
Set-up time for STOP condition	$t_{SU,STO}$	4.0	—	0.6	—	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	1.3	—	μs
Capacitive load for each bus line	C_b	—	400	—	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	—	$0.1V_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	—	$0.2V_{DD}$	—	V

2.3 Measurement result and picture

Measure points are at R907/R906 for I2C_M0_SCL/I2C_M0_SDA.

SYMBOL ADC IIC	Specification		UNIT	Result	Pass/Fail	Figure
	MIN	MAX				
fSCL	0	100	KHz	92.9	Pass	2.3a
tHD;STA	4	-	us	4.84	Pass	2.3b
tLOW	4.7	-	us	7.16	Pass	2.3c
tHIGH	4.0	-	us	6.04	Pass	2.3d
tSU;STA	4.7	-	us	5.56	Pass	2.3e
tHD;DAT	0	3.45	us	2.36	Pass	2.3f
tSU;DAT	250	-	ns	2360	Pass	2.3g
tSU;STO	4	-	us	4.36	Pass	2.3h
tBUF	4.7	-	us	31.24	Pass	2.3i

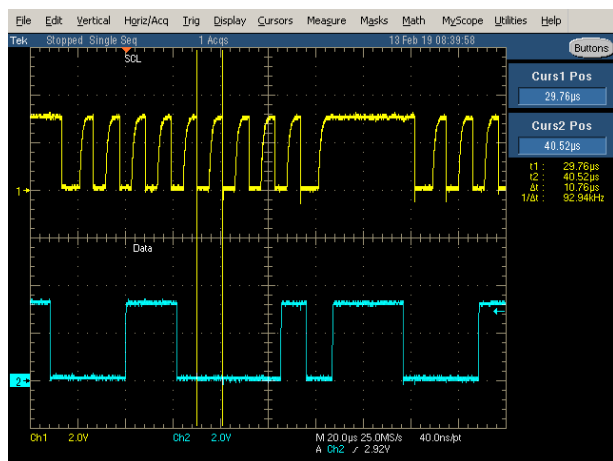


Figure 2.3a: fSCL

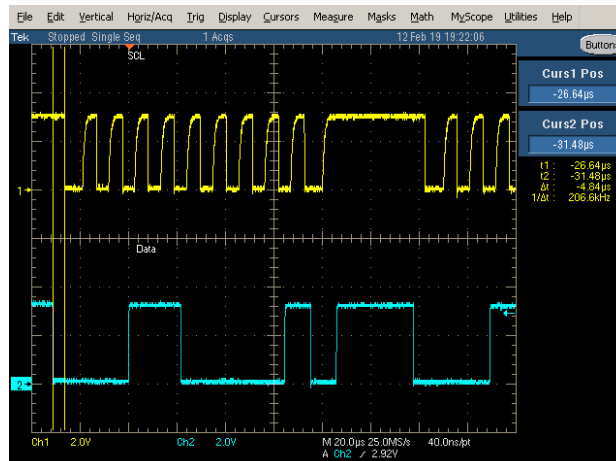


Figure 2.3b: tHD;STA

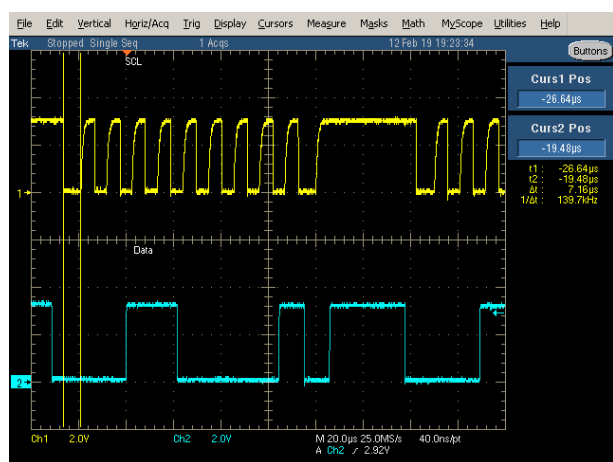


Figure 2.3c: tLOW

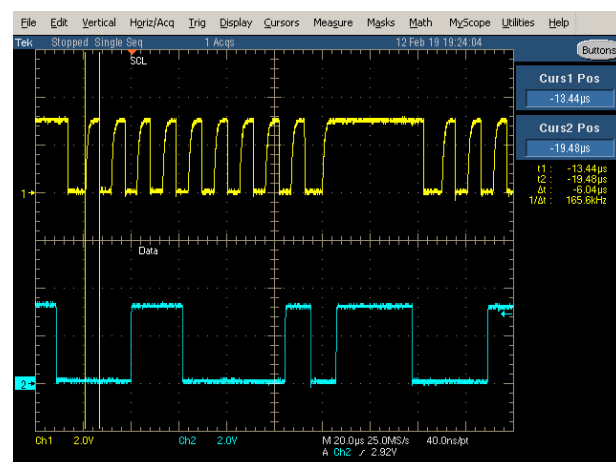


Figure 2.3d: tHIGH

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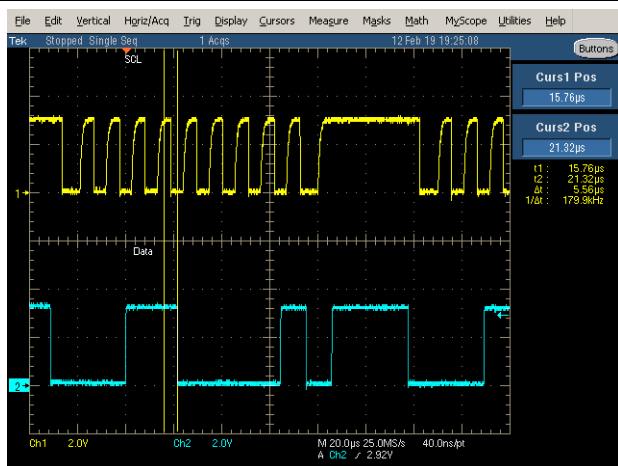


Figure 2.3e: tSU;STA

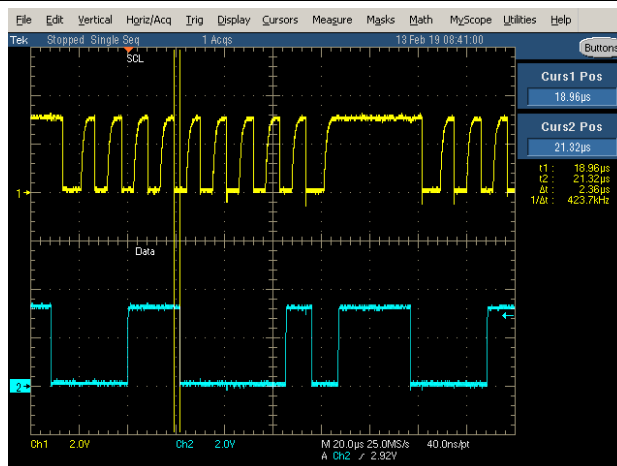


Figure 2.3f: tHD;DAT

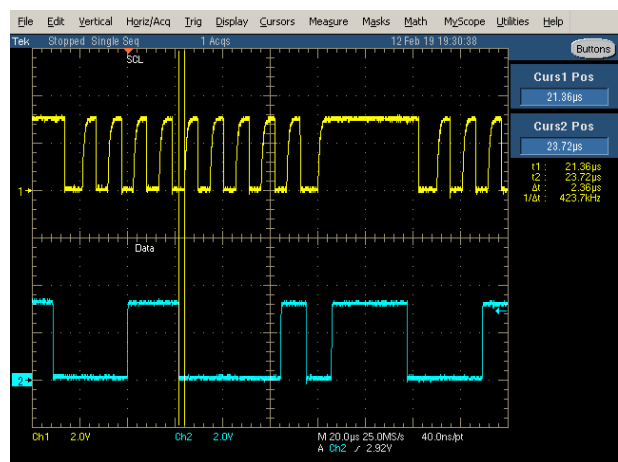


Figure 2.3g: tSU;DAT

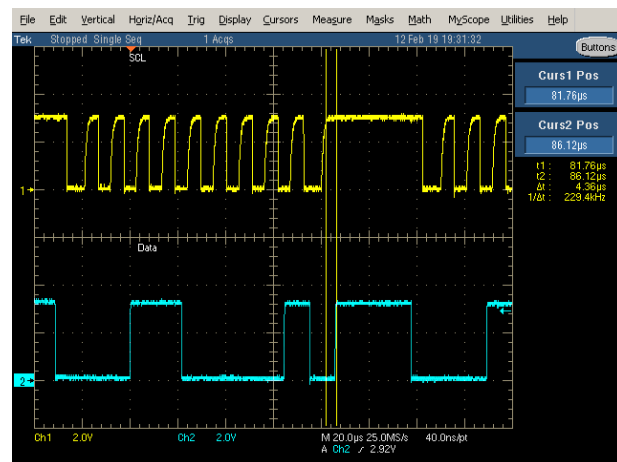


Figure 2.3h: tSU;STO

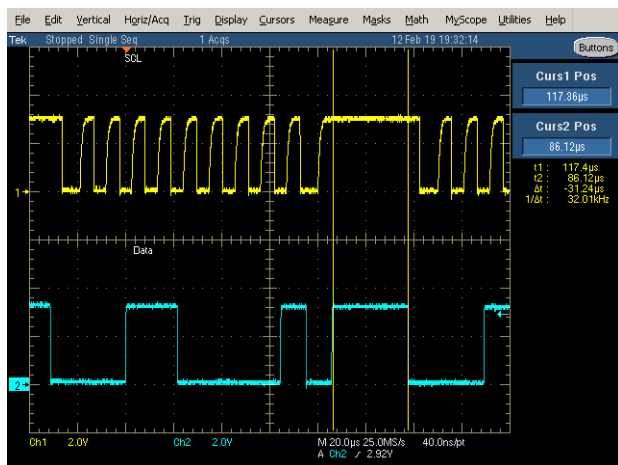


Figure 2.3i: tBUF